Wide Range SET Pulse Measurement

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A method for measuring a wide range of SET pulses is demonstrated. Use of dynamic logic, faster than ordinary CMOS, allows capture of short pulses. A weighted binning of SET lengths allows measurement of a wide range of pulse lengths with compact circuitry. A pulse-length-conservative pulse combiner tree routes SETs from combinational logic to the measurement circuit, allowing SET measurements in circuits that cannot easily be arranged in long chains. The method is applied to add-multiplex combinational logic, and to an array of NFET routing switches, at .35 micron.

Pulses are captured in a chain of Domino Logic AND gates. Propagation through the chain is frozen on the trailing edge by dropping low the second "enable" input to the AND gates. Capacitive loading is increased in the latter stages to create an approximately logarithmic weighted binning, so that a broad range of pulse lengths can be captured with a 10 stage capture chain. Simulations show pulses can be captured which are 1/5th the length of those typically captured with leading edge triggered latch methods, and less than ½ the length of those captured with a trailing edge latch method. After capture, the pulse pattern is transferred to an SEU protected shift register for readout.

64 instances of each of two types of logic are used as targets. One is a full adder with a 4 to 1 mux on its inputs. The other is a 4 x 4 NFET routing matrix. The outputs are passed through buffered XNOR comparators to identify pulses, which are merged in a buffered not-nand (OR) tree designed to avoid pulse absorption as much as possible. The output from each of the two test circuits are input into separate pulse measurement circuits. Test inputs were provided so that the circuit could be bench tested and calibrated. A third SET measurement circuit with no inputs was used to judge the contribution from direct hits on the measurement circuit.

Heavy ions were used with an LET range from 12 to 176. At LET of 21 and below, the very small number of SETs were not significantly higher in the test over the control circuits. At higher LET the test circuit SETs are one or two orders of magnitude greater than for the control circuit. The NFET circuit produces more and slightly longer SETs as expected. But the differences do not appear to be significant enough to modify strategies now used to avoid capture of SETs in chips such as FPGAs. Complete data and graphs will be in the full paper / presentation. In the summary figure below left, "NOCL" is the reference circuit without any input, and number of stages triggered is plotted. Simulation at right shows the smallest pulse captured (stage 2) at about 300 ps. Our conclusion is that the method is promising, but that improvements in the merge network are desirable before applying in a deep submicron process.